said P layer,

said N− drift layer,

a second P base region on said N− drift layer,

a second P+ region on said second P base region to provide an ohmic contact to said second P base region, and

a third electrode which contacts said second shallow P+ region, each of said second electrodes and said third electrodes connected together to provide an emitter connection for said device; the width of said first and second P base regions defining the mesa regions of said IGBT and BJT structures, respectively;

a plurality of insulated gates, each of said insulated gates arranged in a trench configuration and recessed into said N− drift layer and separating said IGBT structures' N+ and P base regions and said BJT structures' P base regions from other ones of said IGBT structures' N+ and P base regions and said BJT structures' P base regions, the portion of a structure located between its adjacent insulated gates defining its mesa region, each of said insulated gates comprising:

a layer of oxide in contact with the N+ and P base region of an IGBT structure when said gate contacts one of said IGBT structures, the P base region of a BJT structure when said gate contacts one of said BJT structures, and said N− drift layer, said layer of oxide forming first and second approximately vertical sidewalls and an approximately horizontal bottom between said sidewalls which contacts said N− drift region,

a conductive material within said trench which connects a voltage applied to the top of said trench to said layer of oxide,

a fourth electrode which contacts said conductive material, each of said fourth electrodes connected together to provide a gate connection for said device, and

a shallow P region in said N− drift layer directly adjacent to said horizontal bottom opposite said conductive material which spans the corners formed at the junctions of said vertical sidewalls and said horizontal bottom to protect said corners from high peak electric fields when said device is reverse-biased; and

an N-type layer which extends above and below the portions of said shallow P region that encroach into said mesa regions, said N-type layer lowering the resistance across said mesa regions that is otherwise increased by said encroachment;

a positive voltage applied to said gate connection forming inversion channels across each of said first P base regions and accumulation channels along the gate sidewalls below said first P base regions which provide conductive paths between each of said N+ regions and said N− drift layer that enable electrons to be injected from said N+ regions into said N− drift layer, said injection of electrons enabling said IGBT structures and said BJT structures to be turned on when the voltage across said collector and emitter is sufficiently high and thereby allowing current to flow between said Collector and said emitter connections via both IGBT and BJT structures, a zero or negative gate voltage eliminating said inversion channels and terminating conduction through the device, said insulated gates recessed into said N− drift layer to a depth sufficient to enable said accumulation channels to enhance the injection of said electrons from said N+ regions to said N− drift layer and thereby lower the forward voltage drop of said IGBT device when compared with an otherwise-identical device having a substantially shallower insulated gate depth,

the ratio of said IGBT structures to said BJT structures determining the saturation current level of said device, said ratio selected to provide a desired saturation current level.

22. The IGBT device of claim **21**, wherein the depth of each of said first P base regions is about 3 μm and the depth of each of said insulated gates is about 10 μm.

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